

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Prior Application: Y. KAMIGAKI et al  
Serial No. 10/377,785  
Filed: March 4, 2003

Group Art Unit: 2826  
Examiner: K. Quinto  
For: SEMICONDUCTOR INTEGRATED CIRCUIT

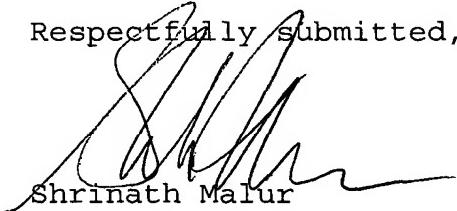
INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents  
Mail Stop Patent Application  
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure, the Applicants inform the Examiner of the documents cited during prosecution of the parent application, USSN 10/377,785.

The Applicants request the Examiner initial and return a copy of the attached PTO-1449 form as an indication that the references have been considered.

Respectfully submitted,  
  
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Registration No. 34,663  
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Date: September 17, 2003

FORM PTO-1449 (REV. 7-80)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. ASA-936-03	SERIAL NO.
<b>LIST OF DOCUMENTS CITED BY APPLICANT</b> <i>(Use several sheets if necessary)</i>				APPLICANT Y. KAMIGAKI et al	
				FILING DATE September 17, 2003	GROUP

**U.S. PATENT DOCUMENTS**

* EXAMINER INITIAL		DOCUMENT	DATE	NAME	CLASS	SUBCLASS	FILING DATE (If Appropriate)
	AA	4,527,259	07/02/85	Watanabe			
	AB	5,763,308	06/09/98	Choi			
	AC	5,467,308	11/14/95	Chang et al			
	AD	5,408,115	04/18/95	Chang			
	AE	5,923,978	07/1999	Hisamune			
	AF	5,357,134	10/1994	Shimoji			
	AG	5,859,459	01/1999	Ikeda			
	AH	4,185,318	01/1980	Engeler et al			
	AI	6,348,387	02/2002	Yu			
	AJ	6,563,151	05/2003	Shin et al			
	AK	5,877,523	03/02/99	Liang et al			

**FOREIGN PATENT DOCUMENTS**

		DOCUMENT	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATIO YES	NO
	AL	0 464664	01/08/92	EP			<input checked="" type="checkbox"/>	<input type="checkbox"/>
	AM						<input type="checkbox"/>	<input type="checkbox"/>
	AN						<input type="checkbox"/>	<input type="checkbox"/>
	AO						<input type="checkbox"/>	<input type="checkbox"/>
	AP						<input type="checkbox"/>	<input type="checkbox"/>

**OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)**

AR		International Conference on Solid State Devices and Materials, Tokyo, 1999, pp. 522-523.
AS		IEEE TRANSACTIONS ON COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY - PART A, Vol. 20, No. 2, June 1997, pp. 182-189.
AT		IEEE ELECTRON DEVICE LETTERS, Vol. 19, No. 7, July 1998, pp. 253-255.

EXAMINER	DATE CONSIDERED
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\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form next communication to applicant.

FORM PTO-1449 (REV. 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. ASA-936-03	SERIAL NO.
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**U.S. PATENT DOCUMENTS**

* EXAMINER INITIAL	DOCUMENT	DATE	NAME	CLASS	SUBCLASS	FILING DATE (If Appropriate)
	AA 5,768,192	6/16/98	Eitan			
	AB 4,554,643	11/19/85	Kuo			
	AC					
	AD					
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	AH					
	AI					
	AJ					
	AK					

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	DOCUMENT	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATIO YES	NO
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	AM					<input type="checkbox"/>	<input type="checkbox"/>
	AN					<input type="checkbox"/>	<input type="checkbox"/>
	AO					<input type="checkbox"/>	<input type="checkbox"/>
	AP					<input type="checkbox"/>	<input type="checkbox"/>

**OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)**

AR		IEDM 94, pp. 57-60.
AS		
AT		

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